AMENDMENT TO THE SPECIFICATION

Please insert the following paragraph at page 1, line 1:

The present patent application is a divisional of Application No.: 09/972,228 filed October 5, 2001, which is currently pending.

Please replace the following paragraphs with the amended paragraphs:

[0002] In the fabrication of semiconductor devices, layers of varying purposes are formed on a semiconductor substrate. One such layer, an inter-layer dielectric (ILD), is deposited and patterned to isolate and support capacitor features such as parallel conductive metal lines. As semiconductor devices and device features decrease in size, the distance between such conductive lines 275, as shown in Fig. 2C, correspondingly decreases. All other factors remaining constant, this results in a higher capacitance (C). For example, given the parallel conductive lines 275 described, capacitance (C) can be viewed as $\frac{k\varepsilon A}{d}$ where (d) is the distance between the conductive lines 275, (A), the area of each conductive line interface, (ε), the permeability of the ILD, and (k), the dielectric constant (a factor of how much effect the ILD material has on capacitor value).

[0004] The dielectric constant (k) noted above has no units of measure. For example, where the dielectric is of a vacuum or air, the dielectric constant (k) is about equal to 1, having no effect on capacitance. However, most intra-layer dielectric materials have a degree of polarity with a dielectric constant (k) above 1. For example, silicon dioxide, a common ILD material, has a dielectric constant generally exceeding about 4. Due to the decreasing size of semiconductor features (e.g., ~~and~~ reduced distance (d) leading to increased capacitance (C)), efforts have recently been made to reduce the dielectric constant (k) of the ILD as a means by which to reduce capacitance (C). That is,

where capacitance (C) is $\frac{k\varepsilon A}{d}$ and all other factors remaining constant, reduction of the dielectric constant (k) can reduce capacitance (C).

[0005] Low dielectric constant (k) materials (i.e. 'low k' materials), such as fluorinated silica glass (FSG), ~~silk~~ SiLK™, and carbon doped oxides (CDO's) have been used to form the ILD, thereby reducing capacitance (C). However, the deposition of 'low k' materials includes a problem of low deposition rate leading to increased semiconductor processing times, also referred to as low thruput.

[0023] With respect to the embodiments described above, the oxygen gas is in an amount that is less than about 5% of the volume taken up by the oxygen and CDO precursor. Additionally, flow rates, in standard cubic centimeters per minute ~~(Sccm)~~ (sccm), for the individual gasses of the gas mixture 160 can be as follows:

Precursor gas flow rate	50-200 ~~Sccm~~ sccm
Background gas flow rate	20-200 ~~Sccm~~ sccm
Oxygen gas flow rate	1.0-20 ~~Sccm~~ sccm